



New Low Profile Low ESL Multi-Anode „Mirror“ Tantalum Capacitor

T.Zedníček, L.Marek, S.Zedníček

AVX Czech Republic s.r.o., Dvorakova 328, 563 01 Lanskroun, Czech Republic
Phone: +420 465 358 126 Fax: +420 465 358 128 e-mail: zednicekt@avx.cz

A B S T R A C T

Traditional tantalum capacitors have been known for their excellent reliability, robustness and stable parameters. This is why conventional tantalum capacitors with counter MnO_2 electrode are still a popular type of capacitor used for long life and high reliability applications. One of the downsides of the MnO_2 electrode system is its higher ESR compared to the polymer type of tantalum capacitors. The multi-anode concept (i.e. use of more node elements within one capacitor body) significantly reduces ESR and is an ideal choice for most demanding applications such as servers and high power telecommunication boards. This paper describes a novel multi-anode configuration that has been developed to reduce the height of the components, reduce manufacturing costs and self inductance ESL. The low ESL extend the working frequency range up to the common DC/DC switching frequency 250 - 500kHz (D case)

Introduction

One common trend in switch-mode power supplies, micro-processors, and digital circuit applications is the reduction of noise while operating at higher frequencies. In order to make these possible components with low Equivalent Series Resistance (ESR), high capacitance and high reliability are required. One way to significantly reduce the ESR of tantalum capacitors has been a multi-anode approach where more anode elements are used within one capacitor body [ref.1- 6] – see Fig.1.

MnO₂ technology provides excellent field performance, environmental stability and high electrical and thermal stress resistance over a wide voltage range from 2.5 to 50 volts. These capacitors are designed for operation in temperatures up to 125°C.

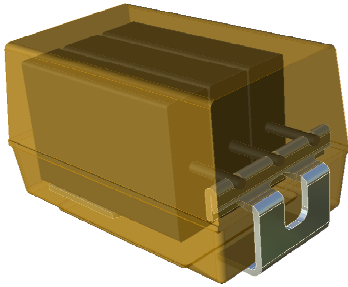
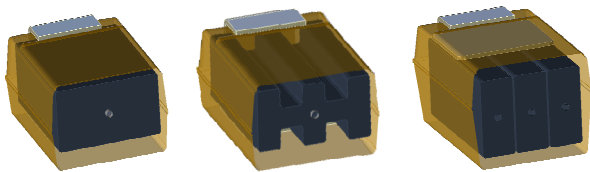


Fig.1. Multi-anode Construction

The overall surface area of a tantalum capacitor anode, particularly its surface-to-volume ratio, is one of the key parameters that define its ESR value - the higher the overall surface area, the lower the ESR.



2a] single 2b] fluted anode 2c] multi-anode

Figure.2. Anode design in cross section

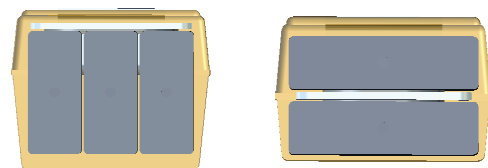
The single anode (Figure 2a) is the standard used for general capacitor designs because of cost versus performance efficiency. A multi-anode design (Figure 2c) offers the lowest possible ESR. Downside of this approach is a higher manufacturing cost compared to a single anode solution. The fluted anode design (Figure 2b) using standard chip assembly

processes is a compromise between low ESR and cost requirements. While the flute design is used in price sensitive low ESR designs, multi-anode concept has been used in applications where low ESR and high reliability is required without compromises such as telecom infrastructure, networking, servers or military/aerospace designs.

Apart from the mentioned differences between single anode, multi-anode and flute anode above there are two additional advantages of the multi-anode concept: 1] Due to a better thermal dissipation of multiple anodes compared to single anodes the multi-anode capacitor can be loaded to higher continuous current and it is also more robust against current surges where heat is dissipated more efficiently. When compared to the single anodes of the same case size the power dissipation of conventional multi-anodes is higher. 2] Compared to the single anode the volumetric efficiency (the active zone) of multi-anodes is lower and that can lead to a presumption that multi-anodes can not reach the same Capacitance times Voltage (CV) factor. In practise, thinner anodes are easier to process and better penetrated by the second MnO₂ electrode system, hence enabling the use of higher CV tantalum powders and therefore in the case of multi-anode capacitors the same or even better CV of the capacitor is achieved.

New Multi-anode Construction

Conventional tantalum multi-anodes on the market mostly use three to five anodes inside one body in a vertical configuration as shown in Fig 3a]. This is practical from the manufacturing point of view, however from the ESR standpoint this solution is inferior to a horizontal layout – see Fig.3b] where thinner flat anodes can reduce the ESR even further. The cost of the multi-anode design grows exponentially with number of anodes. The three anodes currently used in most designs are close to the optimum cost versus ESR ratio.



a] vertical b] horizontal construction

Figure.3. Multi-Anode concept cross section

The individual anodes in the vertical design configuration are connected to the second electrode by a silver glue epoxy to a second electrode lead frame. The same system is used in standard single anode capacitors hence the manufacturing technology is similar to the established process and no major investment into new technology flow is required for the multi-anode design. The horizontal design on the other hand would require a “**solution**” to connection between the anodes and costly modifications of established technology. Hence to date this design has not been used in volume production of the single body multi-anode capacitor. Horizontal designs are used more often in special applications by “stacking” of two or more finished capacitors together by soldering or jigging systems into arrays or modules.

ESR differences between horizontal and vertical configurations are shown in Fig. 4. This example is based on theoretical calculation for D case and it is showing the estimation of ESR for 2, 3 and 4 anode systems in horizontal and vertical configurations. It is can be seen that the two anode horizontal layout has a similar ESR to the three anode system in vertical configuration. The ESR versus cost value is however better for the horizontal multi-anode structure.

Compared to the horizontal the vertical construction has the disadvantage of limited height reduction potential which is currently at 3.5 to 4.5mm. Today, this factor is increasing in importance when miniaturisation of electronics even in applications like telecom infrastructure or military is becoming an issue, where this has not been so in the past.

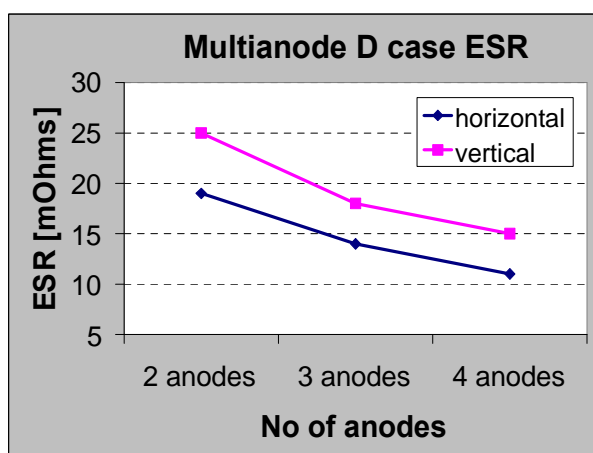
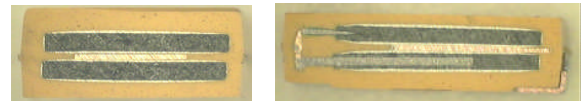
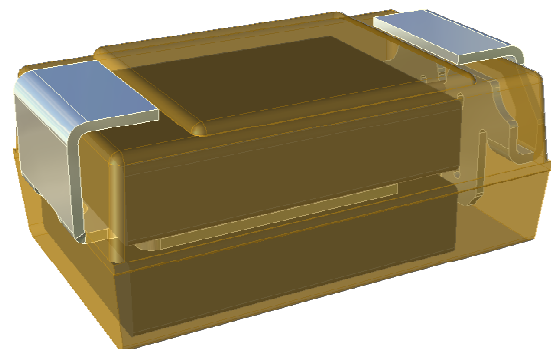


Figure.4. ESR of horizontal and vertical layout

A novel multi-anode construction has been developed using two anodes in horizontal “mirror” configuration – see Fig.5]. The mirror construction uses a modified lead frame shape where the lead frame is in the middle between the two anodes. This configuration solves the connection issues of the horizontal anodes and brings the manufacturing modification cost to acceptable level.



cross section of 2.0mm height 7343case



3D internal construction

Fig.5. Multi-Anode “Mirror” Horizontal Design

The ESR level of the two anode mirror design is slightly inferior to the three vertical anode equivalent however the cost versus performance value is better (2-anode system is cheaper to make compare to 3-anodes). However, the main benefit achieved is that this configuration enables the reduction of component height of multi-anode designs down to 3.1mm 7343-31 D case size and even 2.0 maximum height 7343-20 Y case size in near future. The other advantage of the mirror design is its symmetrical layout which helps to reduce self inductance ESL.

Figure 6. shows a comparison of 22μF 35V typical ESR between the different internal design configurations. As described in the previous chapter, the higher the surface area, the better ESR is achieved. Also the ESR distribution range is much tighter in low ESR designs. Hence the low ESR parts are recommended for circuits with a bank of parallel capacitors due to a more equal load share among the individual capacitors. It should be also noted that there is no direct comparison in the case of vertical multi-anode as it is available in the taller E case size only compared to the other designs made in the

lower D case size. Three vertical D case size anodes in the vertical multi-anode style would show a higher ESR value compared to the E case size data available for this comparison only.

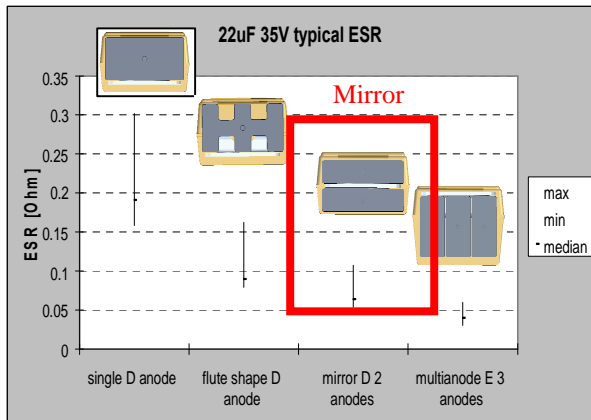


Fig 6. Typical ESR of different internal anode design configurations

The other benefit of mirror design is its symmetrical internal design. The symmetrical construction helps to compensate part of the inductance loop (Fig.7) and thus self inductance ESL is lower compare to a classical lead frame with a pocket. Table 1. shows typical ESL values of a D case size mirror and single anode design capacitor. Catalogue ESL values of D case single anode design is 2.4nH, typical values are around 2.1nH. The mirror design ESL is about 1nH - half of the conventional self inductance. This moves resonance frequency of mirror multi-anodes to higher values – see Fig.8. where resonance frequency of mirror design was measured at 500kHz, the single anode at 340kHz. Capacitance drop with frequency is lower in case of the mirror due to thinner anodes used.

ESL D330/4 [nH]		
sample No.	mirror	single
1	1.06	2.11
2	1.02	2.08
3	0.97	2.25
4	0.95	2.06
5	0.95	1.98
median	0.97	2.08

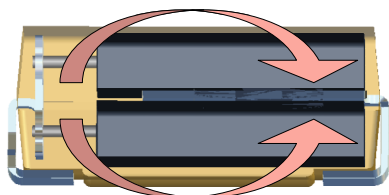


Table 1, Fig.7 ESL of D330/4 capacitor in mirror design and single anode construction

The move of the resonance frequency in mirror design due to the lower ESL significantly improve its working range to today's favorite DC/DC converter switching frequency range 250kHz – 500kHz.

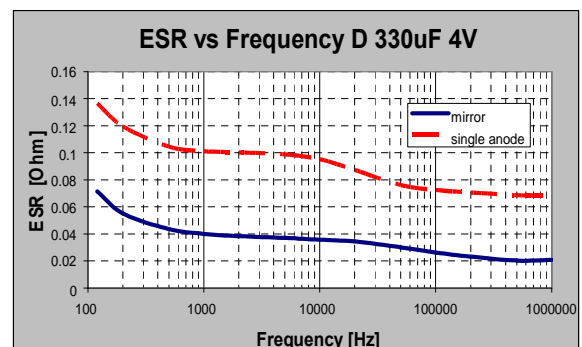
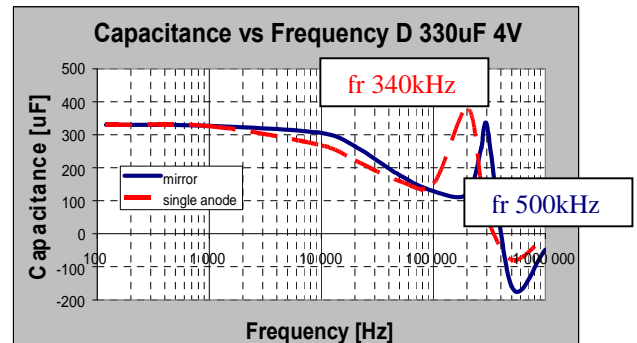


Fig.8. Capacitance and ESR versus frequency behaviour of mirror multi-anode and single anode D case 330μF 4V

The other benefit of the mirror design is in the improved power dissipation capability. The heat generated in anode by ripple current is cooled through leads and tantalum wire by PCB pads. The cooling effect difference is shown in Figure 9.

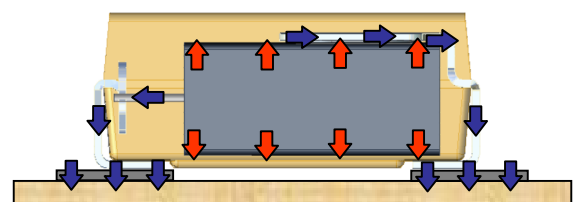


Fig.9a. cooling effect of single anode

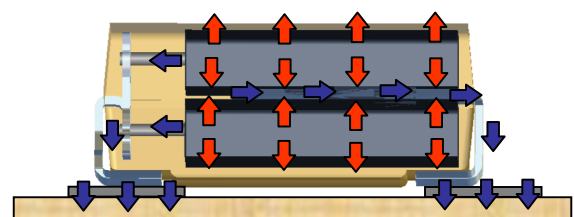


Fig.9b. cooling effect of mirror design

Thus the single anode D case capacitor is capable to continuously dissipate 150mW power compare to 255mW in case of mirror D case. This represent ripple current capability of single design 1.0A (D 330 μ F 10V 150m Ω) with significantly higher 2.7A ripple in the case of mirror design (D 330 μ F 10V 35m Ω).

The mirror type of horizontal multi-anodes can reach capacitance values in TPM D case from 10 μ F to 1000 μ F in voltage 2.5 to 50V with ESR range 25 – 140m Ω . Especially high voltage 35 and 50V capacitors will be attractive for telecommunication application where design height is becoming an important parameter. The capacitance values 10-22 μ F ESR 65-140m Ω on a single 35-50V capacitor are difficult to attain within the 3.1mm maximum height by any other technology.

Summary & Conclusion

A novel "mirror" design approach of horizontal multi-anode tantalum capacitors has been developed. The new construction excels in the following fields:

- better low ESR configuration
- lower profile – D case 7343-31 (3.1mm max height) with potential down to Y case 7343-20 (2.0mm)
- manufacturing cost lower compare to the conventional 3-vertical anode multi-anode design
- lower ESL (symmetrical design) expands significantly the working frequency up to 500kHz (D case)
- significantly higher ripple current capability

Solid Electrolytic Capacitor Assembly using mirror approach has been filed as U.S. Serial No.11/602,451 in the U.S. Patent and Trademark Office on November 20, 2006.

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