TECHNICAL INFORMATION

SOLDER PAD GEOMETRY STUDIES FOR SURFACE MOUNT OF CHIP CAPACITORS*

Kent Wicker & John Maxwell
AVX Corporation
Corporate Research Laboratory
P.O. Box 867
Myrtle Beach, SC 29577

Abstract:

Solder pad geometry for surface mounting chip capacitors were examined visually for three types of defects. Visual defects observed as a function of solder pad geometry were opens, misalignment of chips (rotation) and drawbridges. Geometry of the solder pads was seen to play an important role in the visual defects observed. Of particular importance were the overlap of the pad and the capacitor, the width of solder pads, and the extension of the solder pad outside the capacitor (in the length dimension).

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Introduction

Limited data are available on optimized pad sizes and geometries for the surface mount industry. Data which are available come largely from wave solder applications where an adhesive is first applied to the component. A literature search was made for the range of geometries in use (1, 2, 3, 4, 11) and for surface mount soldering process information (5, 6, 7, 8, 9, 10). Recommendations, where found, were often not explained. Two extreme examples of what was found were: first, a source recommending minimum 50 x 50 mil pads for every chip size; and second, a recommendation using thickness of the capacitor in the formula, which would theoretically require a new pad for each supplier/lot variation encountered.

To address this need, a test board was designed to study several variables of pad geometry. In order to get significant levels of defects for correlations, a method of amplifying defects was used. With this increased defect level, trends were seen between geometric variables and several types of defects.

Although discrete resistors were not tested, much of the discussion should be pertinent for these as well.

Test Procedures

Board design parameters: The test board design with standard component placement is diagramed in Figure 1. Figure 2 shows the dimensioning system for the pads. Table 1 lists the dimensions of the pads on the test board. The board is capable of accommodating many tests by moving components onto pads in columns other than the "standard" configuration shown in Figure 1.

Table 2 lists the experimental parameters of several tests run on the boards. The board was manufactured as a 0.062-in. FR-4 epoxy board with plated Sn/Pb metallization, and as an alumina board with plated Pd/Ag metallization (25 mil thick, Pd/Ag metallization).

An amplification in the incidence of defects was achieved in the batch vapor phase reflow process by employing a vibration of the elevator during the reflow cycle. Initially, this occurred quite by chance. Later, this was deemed necessary to obtain results for correlation analysis. Without the amplification, the rate of defects was insufficient to obtain data in a reasonable time frame. It is worth noting that this same or a similar vibration is common in surface mounting. Conveyors or elevators often have vibrations, and vapor phase reflow is often subject to "oil-canning," which can cause a sudden sharp vibration to the substrates during reflow.

All boards were examined after soldering for visual defects in the solder joints. This data was tallied and entered into a data base for regression analysis.

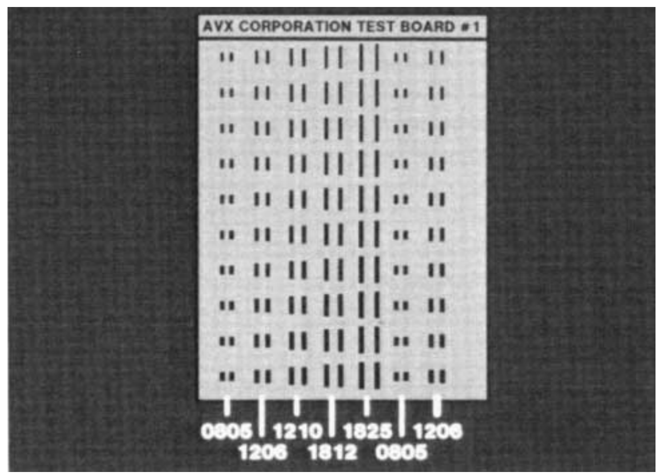
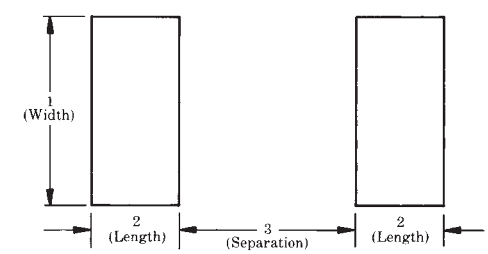


Figure 1. Test Board Layout



Pad Geometry Dimensions

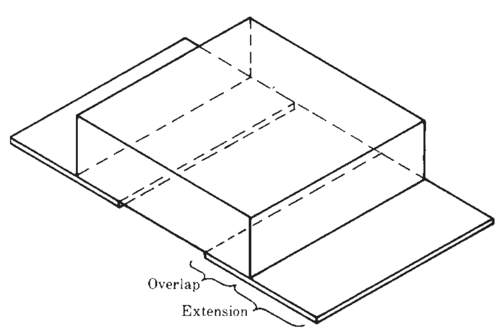


Figure 2. Dimensioning System

		FOR 0805	FOR 1206	FOR 1210	FOR 1812	FOR 1825	FOR 0805	FOR 1206
Row (1)	Dim. 1	0.020	0.020	0.020	0.020	0.020	0.020	0.020
	Dim. 2	0.060	0.070	0.110	0.130	0.260	0.060	0.070
	Dim. 3	0.070	0.110	0.110	0.170	0.170	0.070	0.110
Row (2)	Dim. 1	0.020	0.020	0.020	0.020	0.020	0.020	0.020
	Dim. 2	0.060	0.070	0.110	0.130	0.260	0.060	0.070
	Dim. 3	0.060	0.100	0.100	0.160	0.160	0.060	0.100
Row (3)	Dim. 1	0.030	0.030	0.030	0.030	0.030	0.030	0.030
	Dim. 2	0.060	0.070	0.110	0.130	0.260	0.060	0.070
	Dim. 3	0.060	0.100	0.100	0.160	0.160	0.060	0.100
Row (4)	Dim. 1	0.030	0.030	0.030	0.030	0.030	0.030	0.030
	Dim. 2	0.060	0.070	0.110	0.130	0.260	0.060	0.070
	Dim. 3	0.050	0.090	0.090	0.150	0.150	0.050	0.090
Row (5)	Dim. 1	0.040	0.040	0.040	0.040	0.040	0.040	0.040
	Dim. 2	0.060	0.070	0.110`	0.130	0.260	0.060	0.070
	Dim. 3	0.060	0.100	0.100	0.160	0.160	0.060	0.100
Row (6)	Dim. 1	0.040	0.040	0.040	0.040	0.040	0.040	0.040
	Dim. 2	0.060	0.070	0.110	0.130	0.260	0.060	0.070
	Dim. 3	0.050	0.090	0.090	0.150	0.150	0.050	0.090
Row (7)	Dim. 1	0.040	0.040	0.040	0.040	0.040	0.040	0.040
	Dim. 2	0.060	0.070	0.110	0.130	0.260	0.060	0.070
	Dim. 3	0.040	0.080	0.080	0.140	0.140	0.040	0.080
Row (8)	Dim. 1	0.050	0.050	0.050	0.050	0.050	0.050	0.050
	Dim. 2	0.060	0.070	0.110	0.130	0.260	0.060	0.070
	Dim. 3	0.050	0.090	0.090	0.150	0.150	0.050	0.090
Row (9)	Dim. 1	0.050	0.050	0.050	0.050	0.050	0.050	0.050
	Dim. 2	0.060	0.070	0.110	0.130	0.260	0.060	0.070
	Dim. 3	0.040	0.080	0.080	0.140	0.140	0.040	0.080
Row (10)	Dim. 1	0.050	0.050	0.050	0.050	0.050	0.050	0.050
	Dim. 2	0.060	0.070	0.110	0.130	0.260	0.060	0.070
	Dim. 3	0.030	0.070	0.070	0.130	0.130	0.030	0.070

Table 1. Pad Dimensions On Test Board #1 (In Inches)

Defect Categorization

Visual defects were categorized into three types:

Misalignment of the Component (Type 1): In this paper, a misaligned part is arbitrarily chosen as a rotation greater than 15º from the centerline axis of the pads. Figure 3 illustrates this. While this is not necessarily a functional defect, it can be important for strength of the solder joint, and reliability under temperature cycling. Each application requires an assessment of the acceptable limits for this defect.

Opens (Type 2): For this paper, an open is a chip which has pulled off one solder pad and onto the other pad. Figure 4 illustrates this. Opens result from an imbalance of forces, just as drawbridges.

Drawbridging or Tombstoning (Type 3): A drawbridge occurs when a capacitor flips up to a vertical or near vertical position (see Figure 5). Smaller capacitors are more susceptible to drawbridging and the 0805 size in particular. Wetting forces and solder paste tackiness are involved, as well as the force of gravity.

Factors Other Than Pad Design Which Affect Visual Defects

During the course of this work and from discussions with others involved in this area, several variables other than pad geometry were seen to affect visual defects. These are listed, most without supporting data, to assist in trouble-shooting in the field:

Misalignment:

1) Poor design of conductive path metallization - In a circuit, the conductive path can wick solder away from the component and actually move the component with the solder. This occurs particularly where a wide path leads away from the component. Necking of the conductive path at the component will largely eliminate this problem. Solder dams are also effective when placed properly.

2) Solder dams improperly placed - These can contribute to drawbridging when, for example, a solder dam exists on one side of the component but not the other.

3) Poor test pad placement - This is similar to the conductive path discussion. A relatively large area of metallization can attract the solder and then the component by the same wicking action.

4) Solderability - This can cause an imbalance of forces and contribute to opens.

Opens: The parameters other than pad geometry are the same as for misalignment, but are listed again here for clarity:

1) Poor design of conductive path metallization

2) Solder dams improperly placed

3) Poor test pad placement

4) Solderability

Drawbridges:

1) Center of gravity of the chip capacitor too high - A discrete capacitor with a high center of gravity is easily drawbridged. This is due to the large wetting force moment arm relative to the moment arm for rotation.

2) Component weight - Extremely lightweight capacitors were seen to drawbridge frequently. This data will be discussed elsewhere in this paper.

RUN	ID #	BOARDS	COMPONENTS USED	SOLDER PASTE THICKNESS (Mil)	REFLOW PROCEDURE	SOLDER TYPE	BOARD TYPE	COMMENTS
A		15	Experimental 0805 Experimental 1206	4.5-6.0	Vapor Phase (FC 71) 10 sec.	60/40	Alumina	
B		30	Pd/Ag 0805 1206 1210 1812 Experimental 1206	4.5-6.0	Vapor Phase (FC 71) 10 sec.	60/40	Alumina	Placed experimental 1206 parts on pads intended for 0805 size parts
C		30	Pd/Ag 0805 1206 1210 1812	4.0-5.0	Vapor Phase (FC 71) 1 min.	60/40	Alumina	
D		30	Pd/Ag 0805 1206 1210 1812	1.0-13.5	Vapor Phase (FC 71) 1 min.	60/40	Alumina	
Y	100	10	Pd/Ag 0805-2 cols 1206-2 cols 1210-1 col.	5.0-10.0	Vapor Phase (FC 70) 40 sec.	63/37	FR-4	No vibration
Y	200	24	Pd/Ag 0805-2 cols 1206-2 cols 1210-1 col.	5.0-10.0	Infrared	63/37	FR-4	No vibration
Z	100	10	Experimental 0805 1206	5.0-10.0	Infrared	63/37	FR-4	No vibration

Table 2. Summary of Experimental Parameters for Test Board Fabrication

3) Solder masking too thick under discrete capacitors. This can cause unequal contact to the metallization or solder. The chip becomes essentially a small seesaw. Bumpy metallization could easily cause this as well.

4) Inadequate force during placement - Insufficient force during placement causes chip to sit high on solder, often with uneven amounts of solder in contact with the terminations. This was easily observable from experience in hand placement of capacitors.

5) Poor centering of chips on pads - This was not studied in a controlled manner at time of publication.

6) Solder laydown too heavy - This would relate to the moment arm argument discussed above.

7) Uneven heating of solder during reflow - This would result in one end wetting to molten solder before the other.

8) Poor solderability of the termination - This directly affects the wetting forces and so can cause imbalances in the forces, resulting in drawbridging.

Results

Table 3 shows a summary of the regression analysis. To understand the results, each type of visual defect is discussed separately below.

1) Misalignment: In general, misalignment correlates to the overlap and separation. This correlation is very strong in the Pd/Ag chips. These capacitors have a 5-sided or wrap-around thick film termination. From the chip dimensions shown in Table 4, it seems that when the overlap is less than the land length, the chip has a greater tendency to misalign. This implies that there may be a

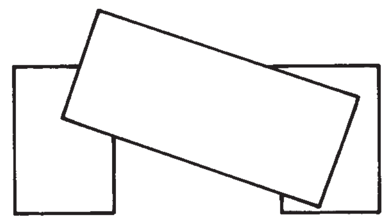


Figure 3. Misalignment

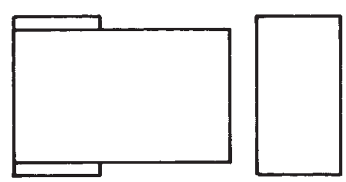


Figure 4. Open

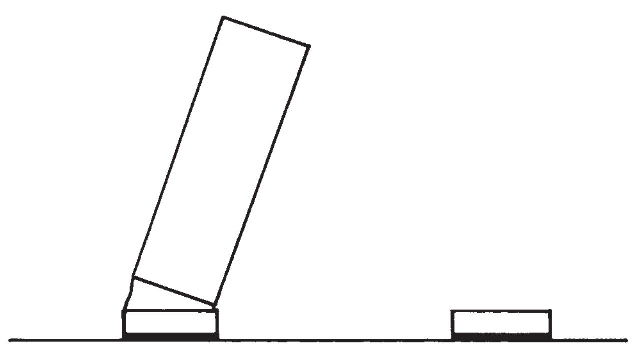


Figure 5. Drawbridge

"critical" overlap for Pd/Ag chips which the number of defects increases dramatically. Figure 7 illustrates this idea using data on Type 1 defects vs. overlap from the runs B, C, and D. The other possibility comes from considering the overlap to extension ratio of the parts, as shown in Figure 8 for the same data. When O/E becomes small, the wetting pull from the extension may cause misalignment due to the large imbalance of force. It is not possible to discriminate without further testing. Wherever O/E showed a possible effect on the data, it was noted in Table 3.

In this work, a distinction was made between overlap and separation because overlap is a function of the chip length and separation is not. For these correlations, the overlap and separation were equivalent because the same chips were used.

A separate experiment was run to determine the effect of pad width on misalignment defect rate. Photograph 1 shows a board which was reflowed with 1206 components on very wide pads relative to part width, and 1210 components on narrow pads. The incidence of misalignment was approximately four times greater for 1206 parts on wide pads. This is not conclusive, because component weight could be a factor. A limiting factor for narrowing the pads is that solder joint shear force decreases with decreasing pad size.

2) Opens: The incidence of opens showed a strong correlation to overlap and separation. Figure 9 shows a graph of opens vs. separation for 0805 Pd/Ag and Figure 10 shows open vs. overlap for 1210 Pd/Ag parts. The coefficients of determination (r^2) for these regressions are very high. The trends showed defects increasing with increasing extension, and decreasing defects as overlap and O/E increased. The same correlations were not evident in the 1206 data.

Mention is made here that in several cases, the extremely small pads in the top two rows of the board

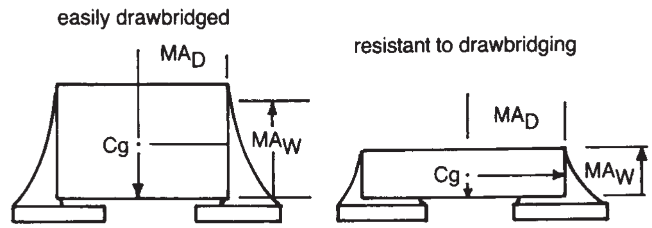


Figure 6. Moment Arms for Forces of Rotation and Wetting for Forces of Two Different Chips

MA_D = Moment Arms for Drawbridging

MA_W = Moment Arm For Wetting

sometimes gave an anomalous point in the plots. This may have caused several regressions not to show a trend where one would have been expected.

3) Drawbridges: A strong trend occurred for drawbridging incidence as a function of overlap and extension. 0805 parts were the only size where appreciable drawbridging was seen.

In addition, some runs were made with the lightweight experimental parts (see Table 4). These chips drawbridged quite easily. When the 1206 components were reflowed under the same conditions using the column of pads intended for 0805 components, drawbridging was reduced to near zero even with the vibration present and using the full range of ten pad geometries. This data was not analyzed in depth, but is given as an indication that the overlap dimension is capable of controlling drawbridging.

As a result of the above work, pad recommendations were developed for 0805, 1206, and 1210 components. These are shown in Figure 11. The development of these pad designs incorporated practical experience of the AVX Surface Mount Laboratory, as well as the results of the above work.

COMPONENT TYPE	DEPENDENT VARIABLE	INDEPENDENT VARIABLE	RELATIONSHIP	BEST FIT REGRESSION	COEFFICIENT OF DETERMINATION (r^2)
0805 Pd/Ag	Misalignment (Type 1)	Overlap Overlap/ Extension Separation	As overlap , defects As O/E , defects As sep. , defects	$5.3x10^5X^3-2.5x10^3X^2+2.8x10^2X-.02$ (discussed in report) $-6.6x10^3X^3+1.1x10^3X^2-5.5x10X+.84$	0.796 0.796
1206 Pd/Ag	Misalignment (Type 1)	Overlap Overlap/ Extension Separation	As overlap , defects As O/E , defects As sep. , defects	$1.3x10^2X^2-7.2X+.095$ (discussed in report) $3.5x10^2X^2-5.4X+.20$	0.681 0.673
1210 Pd/Ag	Misalignment (Type 1)	No Correlations Found			
0805 Pd/Ag	Opens (Type 1)	Overlap Separation O/E	As overlap , defects As sep. , defects As O/E , defects	$-7.5x10^4X^3+5.5x10^3X^2-1.3x10^3X+1.1$ $-9.6x10^5X^4+1.9x10^5X^3-1.3x10^4X^2+3.9x10^2X-4.3$	0.902 0.927
1206 Pd/Ag	Opens (Type 2)	Overlap Separation	As overlap , defects As sep. , defects	$-1.5x10^5X^3+1.1x10^4X^2-2.4x10^2X+1.8$ $-2.5x10^5X^3+3.1x10^4X^2-1.7x10^3X+35.7$	0.951 0.963
1210 Pd/Ag	Opens (Type 2)	Overlap Separation	As overlap , defects As sep. , defects	$1.9x10^3X^2-9.6x10X+1.2$ $4.7x10^2X^2-6.9x10X+2.5$	0.870 0.870
0805 Pd/Ag	Drawbridges (Type 3)	No Correlations Found			

Table 3. Summary of Regression Analysis Results

CHIP TYPE/SIZE	MEAN LENGTH (in.)	MEAN WIDTH (in.)	MEAN THICKNESS (in.)	MEAN LAND LENGTH (in.)	MEAN COMPONENT WEIGHT (g.)
Pd/Ag					
0805	0.086	0.052	0.030	0.015-0.025	0.010
1206	0.130	0.066	0.031	0.015-0.025	0.021
1210	0.124	0.095	0.055	0.015-0.025	0.050
1812	0.175	0.125	0.038	0.015-0.025	-
Experimental					
0805	0.087	0.054	0.029	end-only terminations	0.006
1206	0.118	0.055	0.029	end-only terminations	0.008

Table 4. Dimensions of Chips Used

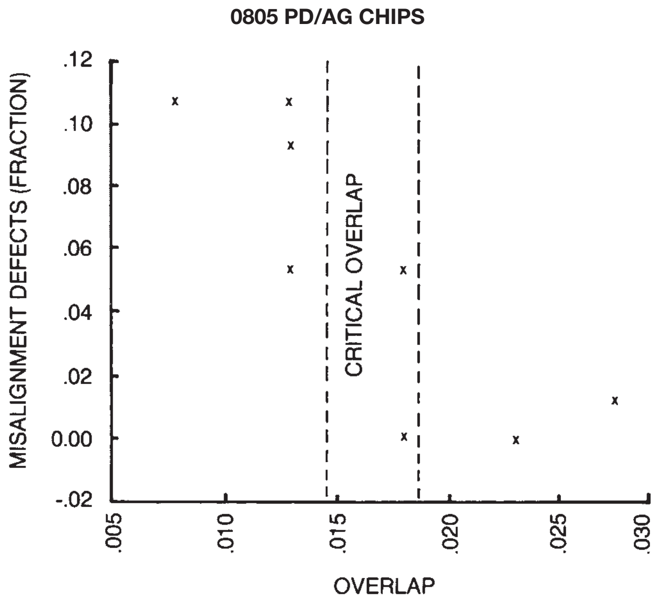


Figure 7. Critical Overlap Concept

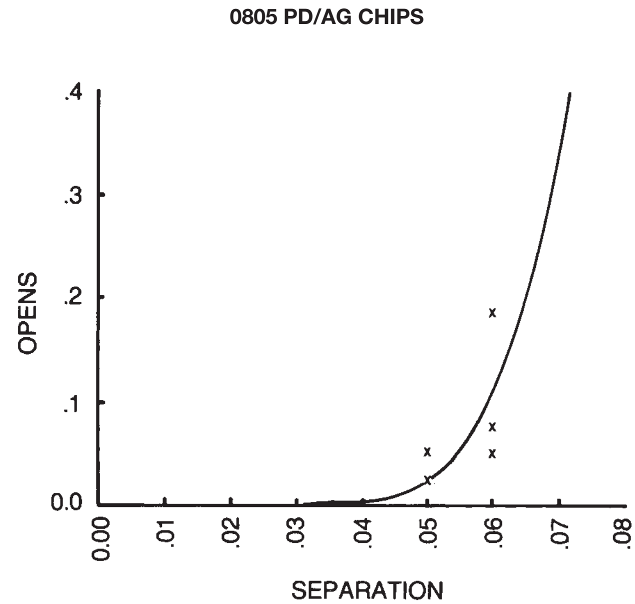


Figure 9. Opens vs. Separation (0805 Pd/Ag)

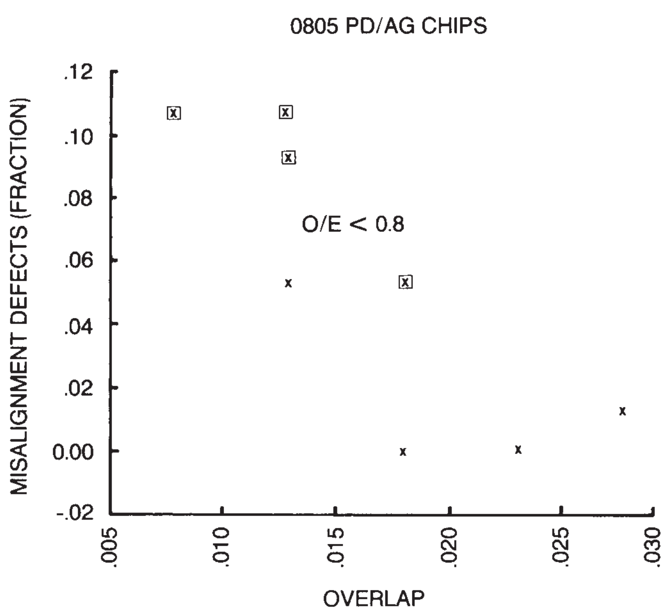


Figure 8. Overlap/ Extension Effect

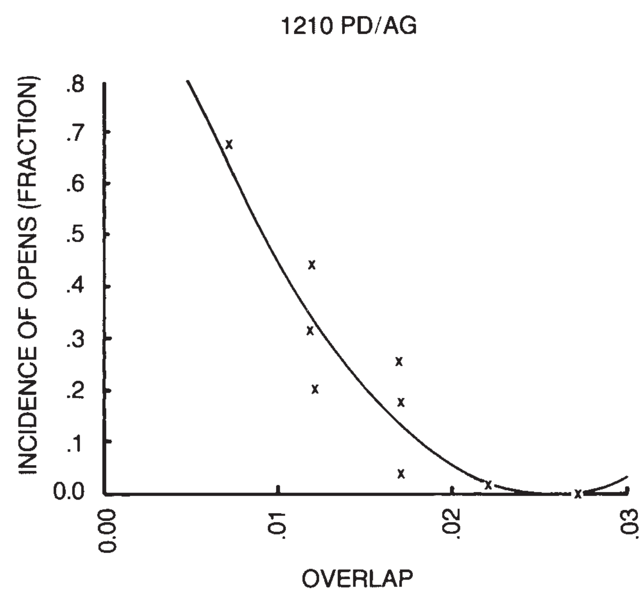


Figure 10. Opens vs. Overlap (1210 Pd/Ag)

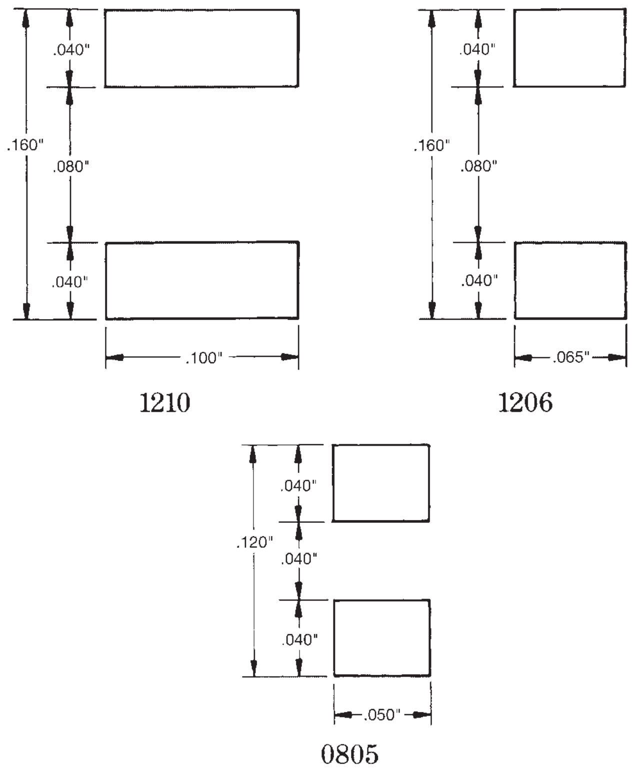
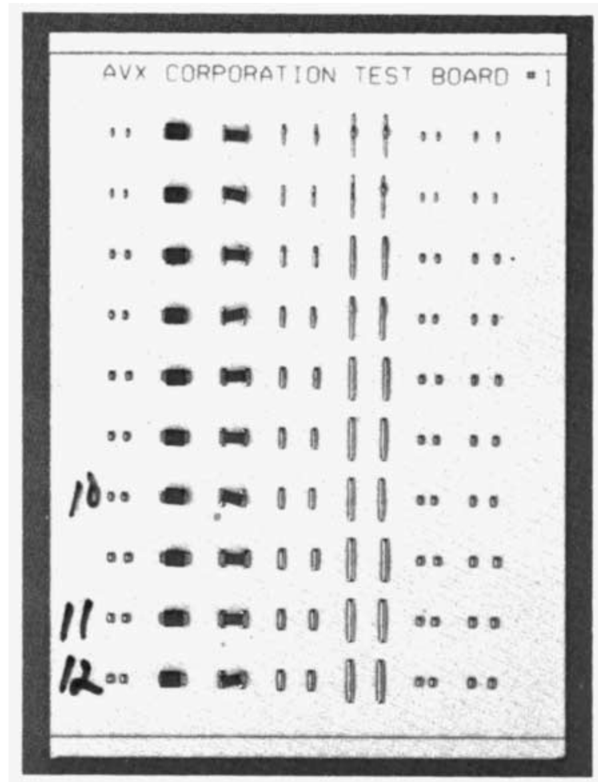


Figure 11. Recommended Pad Dimensions



Photograph 1. Misalignments Due to Pad Width

Conclusions

1) Overlap and separation of the solder pads were the dominant factors for all three types of visual defects.

2) Overlap was inversely related to the incidence of defects for all three defect types. Greater overlap caused less defects.

3) Separation of the solder pads was positively related to the incidence of defects for all three defect types. Large separation causes more defects.

4) Possible correlation exists between solder pad width and the incidence of misalignment.

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USA

AVX Myrtle Beach, SC
Corporate Offices
Tel: 843-448-9411
FAX: 843-626-5292

AVX Northwest, WA
Tel: 360-699-8746
FAX: 360-699-8751

AVX North Central, IN
Tel: 317-848-7153
FAX: 317-844-9314

AVX Mid/Pacific, MN
Tel: 952-974-9155
FAX: 952-974-9179

AVX Southwest, AZ
Tel: 480-539-1496
FAX: 480-539-1501

AVX South Central, TX
Tel: 972-669-1223
FAX: 972-669-2090

AVX Southeast, NC
Tel: 919-878-6223
FAX: 919-878-6462

AVX Canada
Tel: 905-564-8959
FAX: 905-564-9728

EUROPE

AVX Limited, England
European Headquarters
Tel: ++44 (0) 1252 770000
FAX: ++44 (0) 1252 770001

AVX S.A., France
Tel: ++33 (1) 69.18.46.00
FAX: ++33 (1) 69.28.73.87

AVX GmbH, Germany - AVX
Tel: ++49 (0) 8131 9004-0
FAX: ++49 (0) 8131 9004-44

AVX GmbH, Germany - Elco
Tel: ++49 (0) 2741 2990
FAX: ++49 (0) 2741 299133

AVX srl, Italy
Tel: ++390 (0)2 614571
FAX: ++390 (0)2 614 2576

AVX Czech Republic, s.r.o.
Tel: ++420 (0)467 558340
FAX: ++420 (0)467 558345

ASIA-PACIFIC

AVX/Kyocera, Singapore
Asia-Pacific Headquarters
Tel: (65) 258-2833
FAX: (65) 350-4880

AVX/Kyocera, Hong Kong
Tel: (852) 2-363-3303
FAX: (852) 2-765-8185

AVX/Kyocera, Korea
Tel: (82) 2-785-6504
FAX: (82) 2-784-5411

AVX/Kyocera, Taiwan
Tel: (886) 2-2696-4636
FAX: (886) 2-2696-4237

AVX/Kyocera, China
Tel: (86) 21-6249-0314-16
FAX: (86) 21-6249-0313

AVX/Kyocera, Malaysia
Tel: (60) 4-228-1190
FAX: (60) 4-228-1196

Elco, Japan
Tel: 045-943-2906/7
FAX: 045-943-2910

Kyocera, Japan - AVX
Tel: (81) 75-604-3426
FAX: (81) 75-604-3425

Kyocera, Japan - KDP
Tel: (81) 75-604-3424
FAX: (81) 75-604-3425

Contact:

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